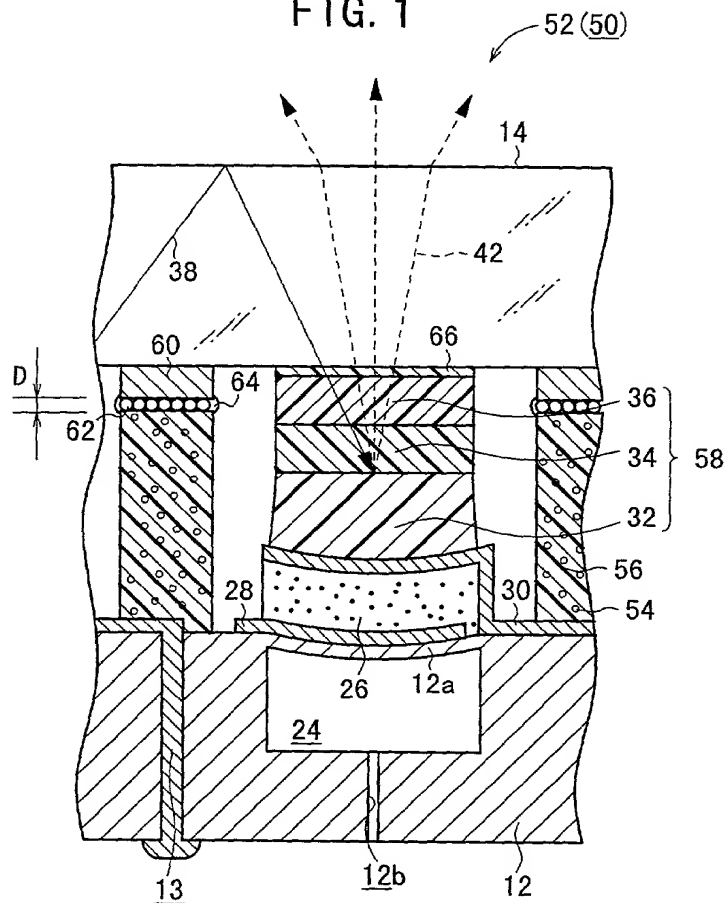


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FIG. 1



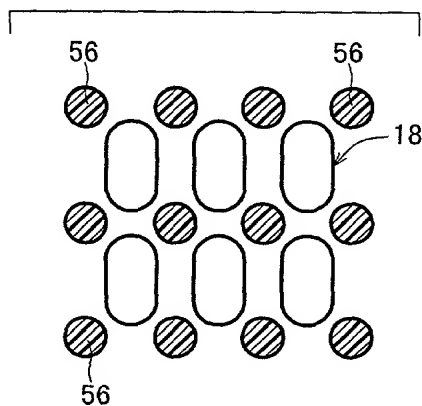
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FIG. 2



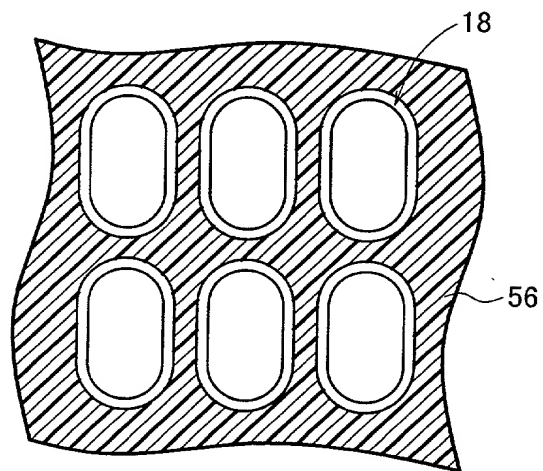
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FIG. 3



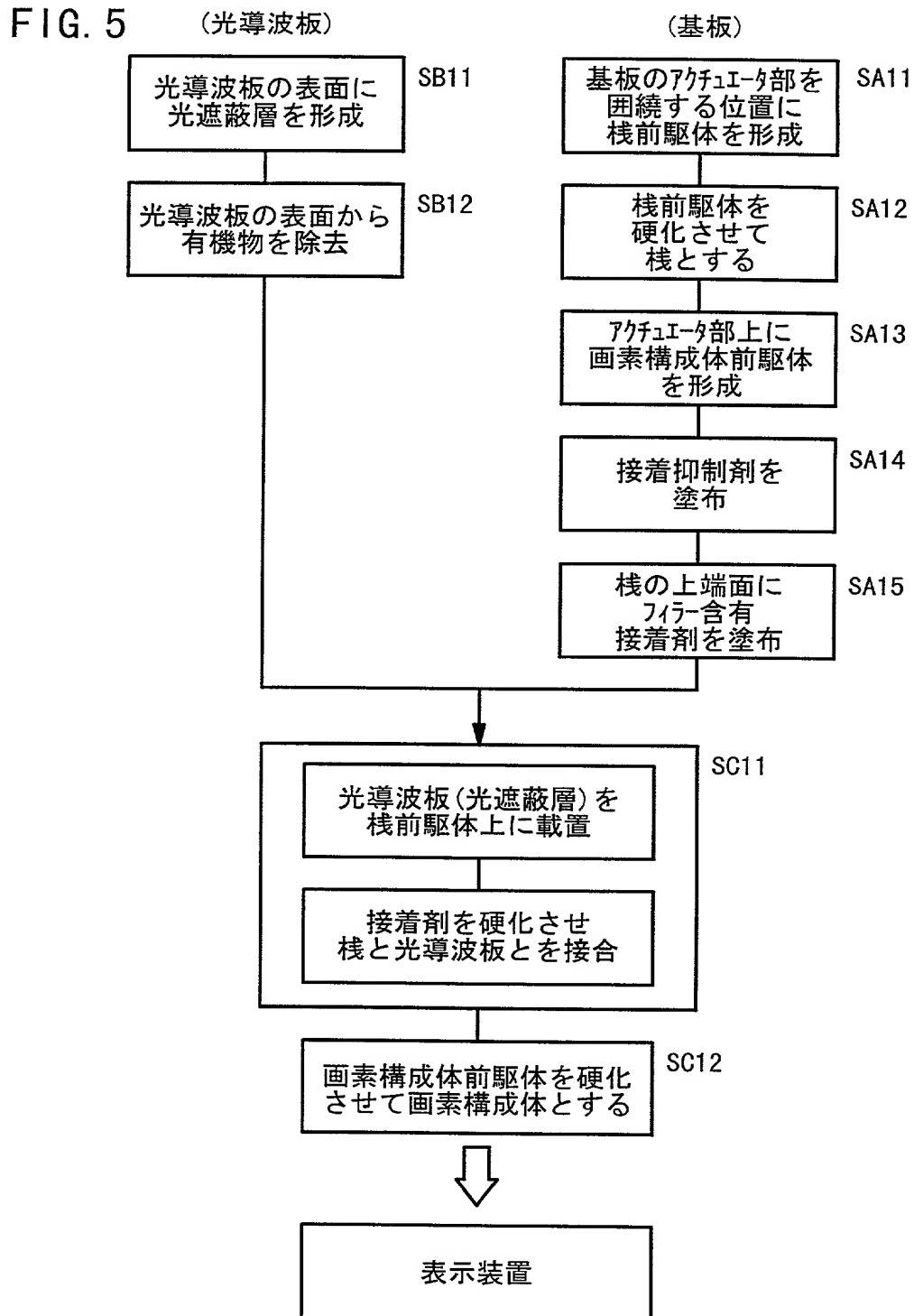
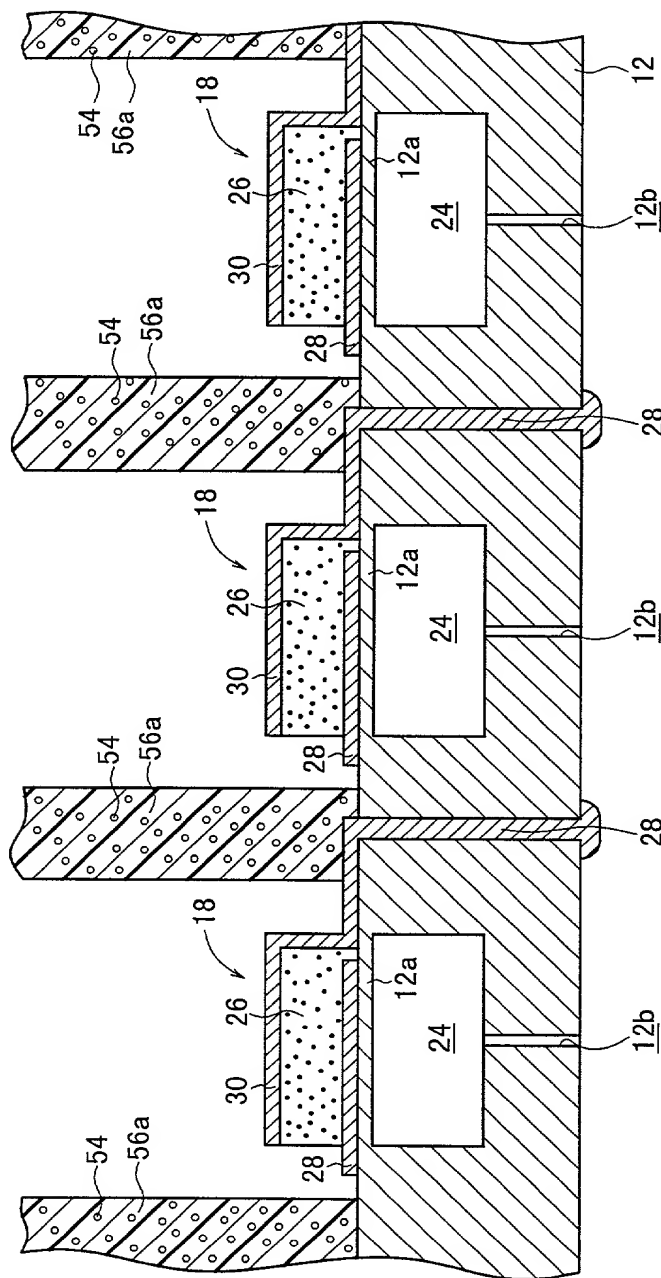


Figure 1 is a cross-sectional view of a semiconductor device 100. The device consists of a substrate 12 with a gate stack 13. The gate stack 13 includes a gate 12a and a channel 12b. The gate 12a is connected to a source/drain region 24. The channel 12b is connected to a contact 26. The contact 26 is covered by a passivation layer 30. The device is divided into three identical vertical sections by a trench 28. The trench 28 is filled with a material 28. The device is labeled 100.



This diagram shows a cross-section of a semiconductor device with several stacked layers. From top to bottom, the layers are labeled as follows:

- Top Layer Group (58a):** Consists of three sub-layers: 36a (topmost), 34a (middle), and 32a (bottom).
- Layer 54:** Located below layer 32a.
- Layer 56:** Located below layer 54.
- Layer 18:** A thick layer below 56, featuring a hatched pattern.
- Layer 30:** Below layer 18, containing a dotted pattern.
- Layer 28:** A thin layer directly beneath layer 30.
- Bottom Layer (12):** The base substrate, shown with diagonal hatching.

On the right side of the device, there are two rectangular blocks, each labeled with "26", "12a", and " $\overline{24}$ ". These blocks are positioned between the bottom layer 12 and the upper layers. Small vertical features, labeled 12b, are located at the interfaces between the bottom layer 12 and the blocks. On the left side, there are small circular features labeled 13, which appear to be vias or contacts passing through the layers.

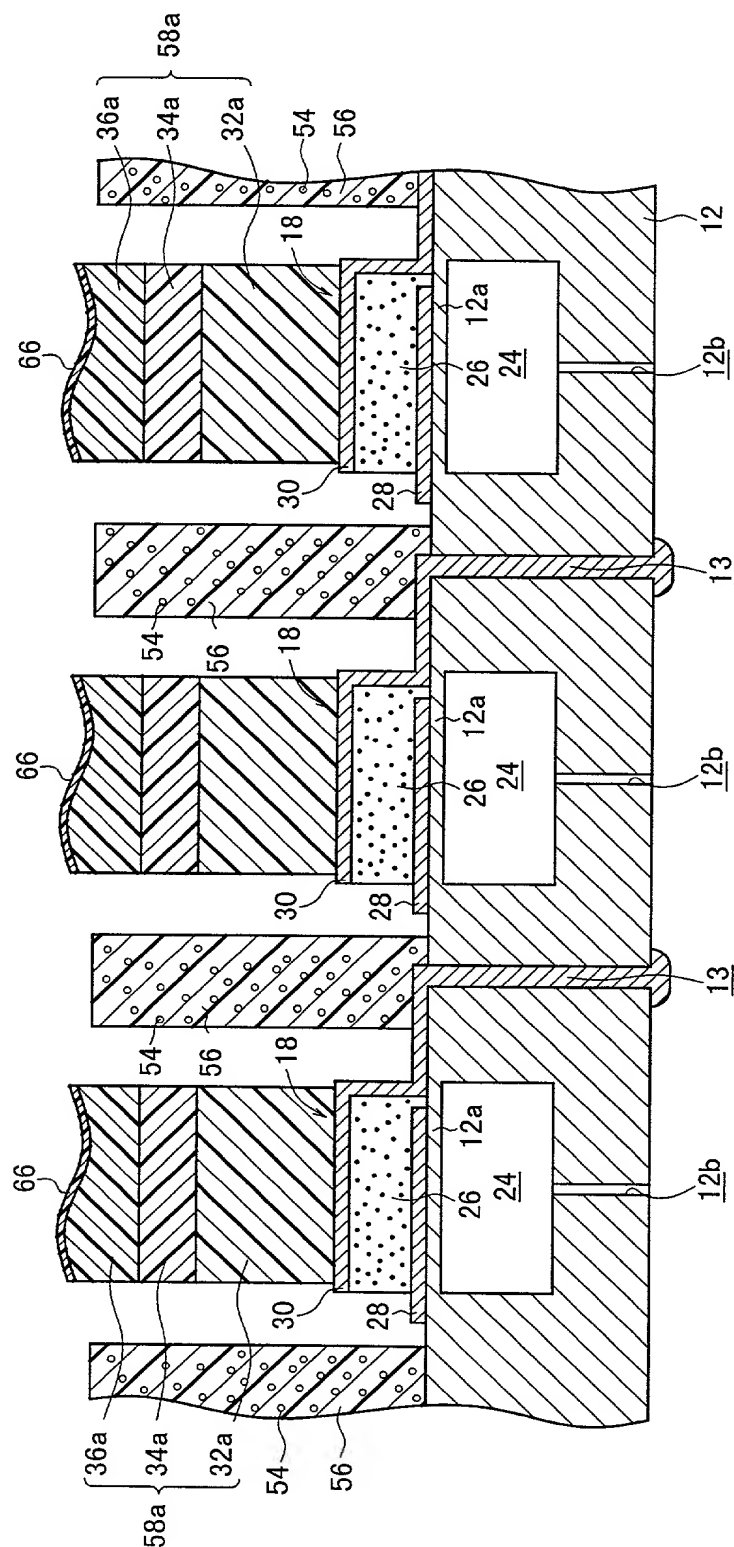


FIG. 10

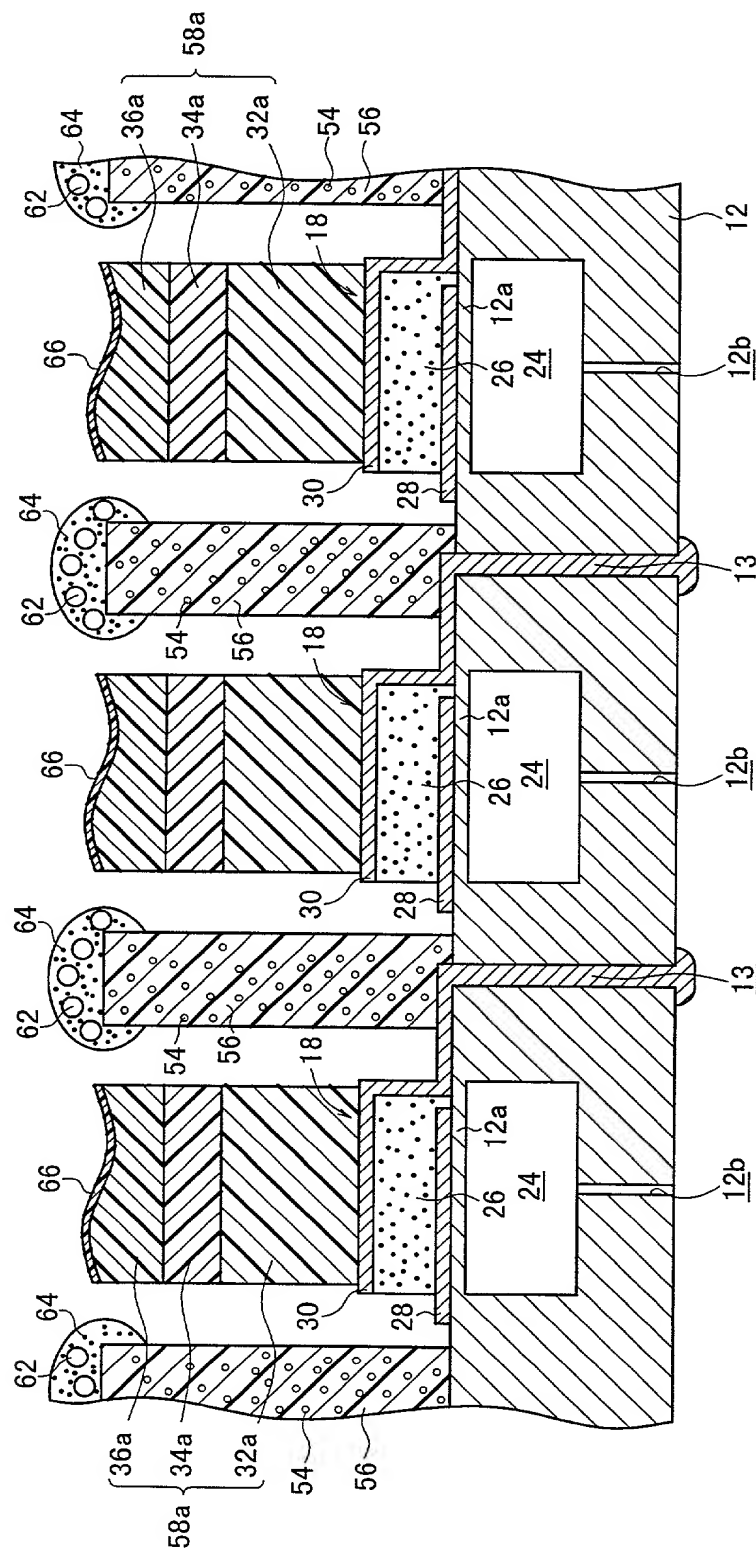


FIG. 11

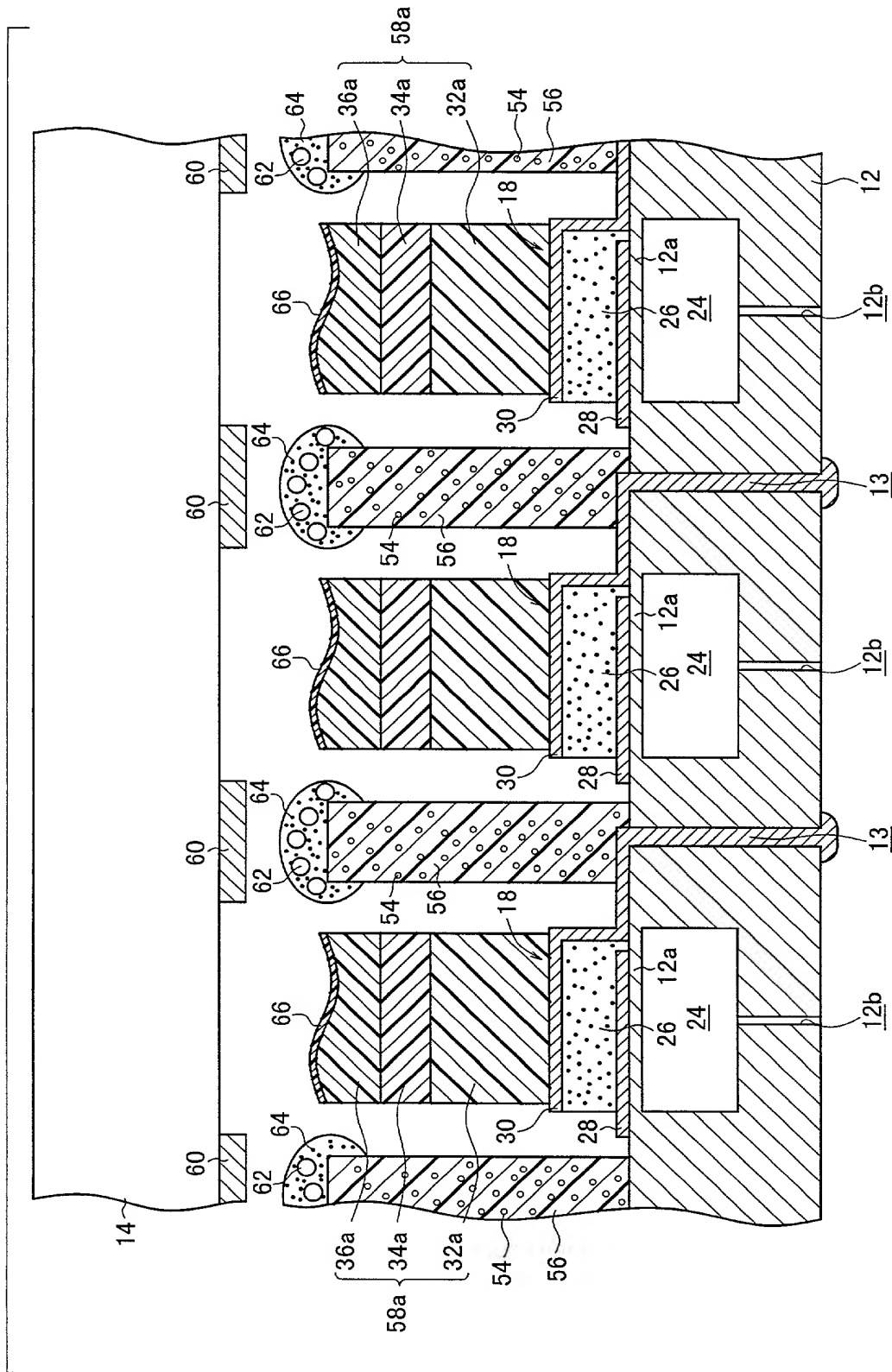


FIG. 12

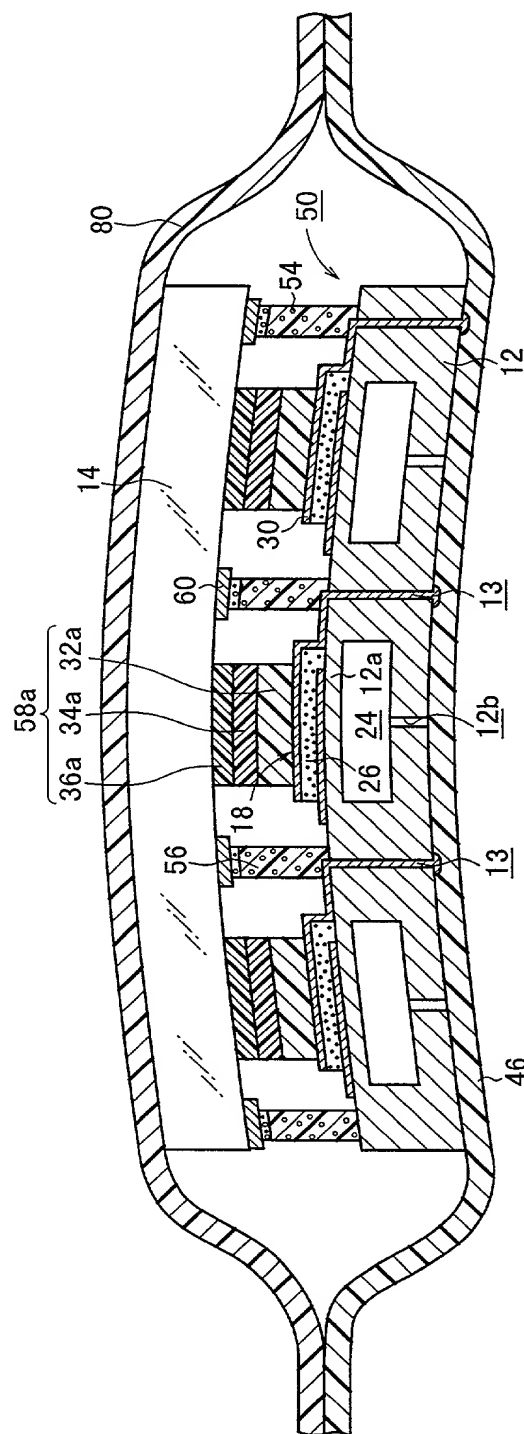
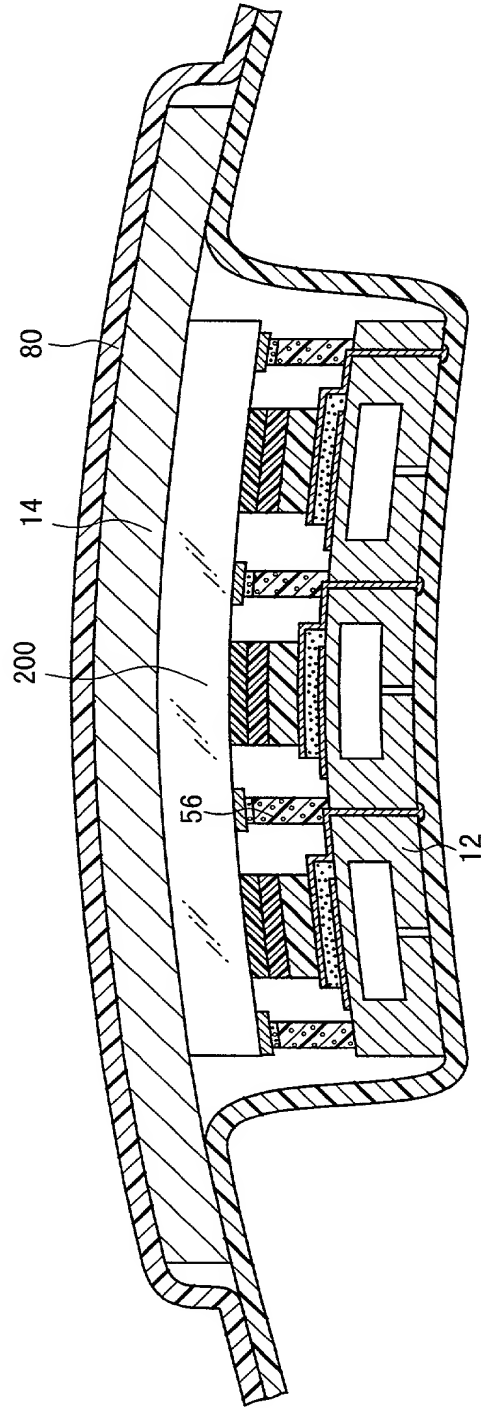


FIG. 13



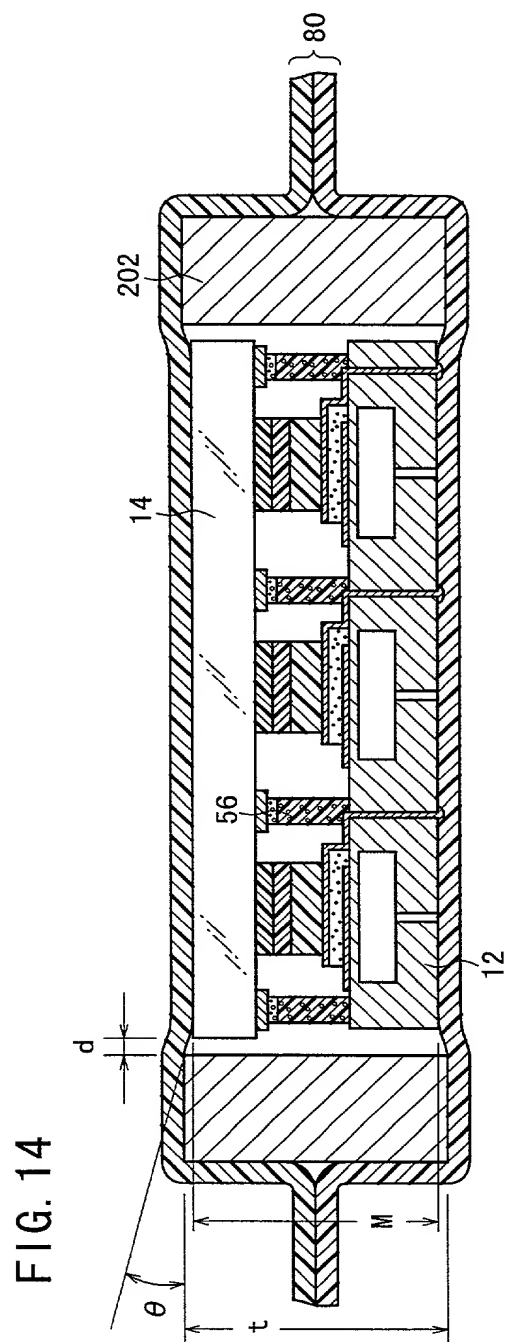


FIG. 15

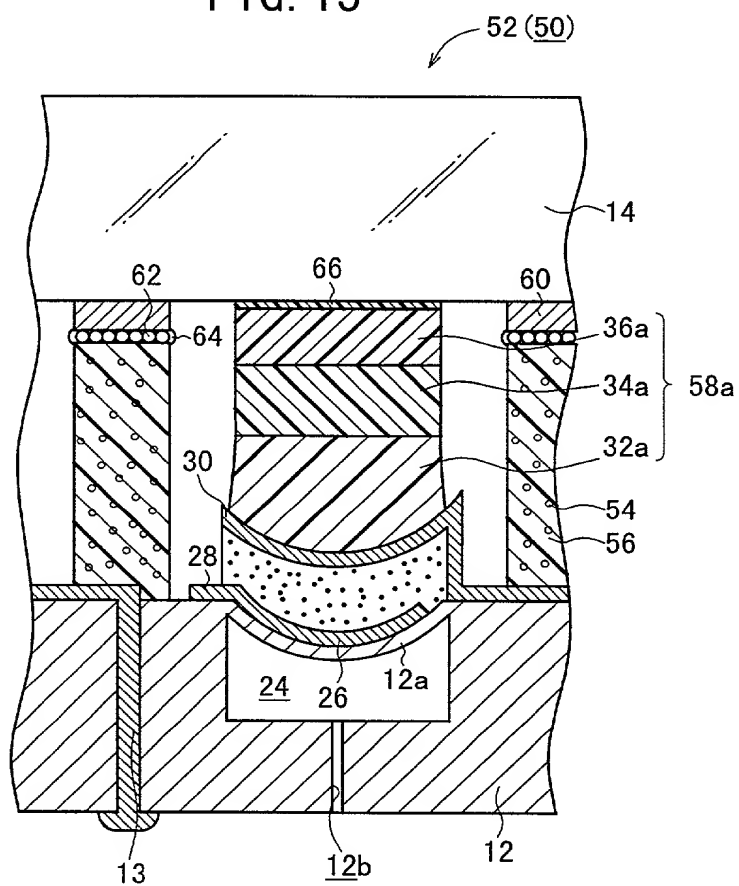
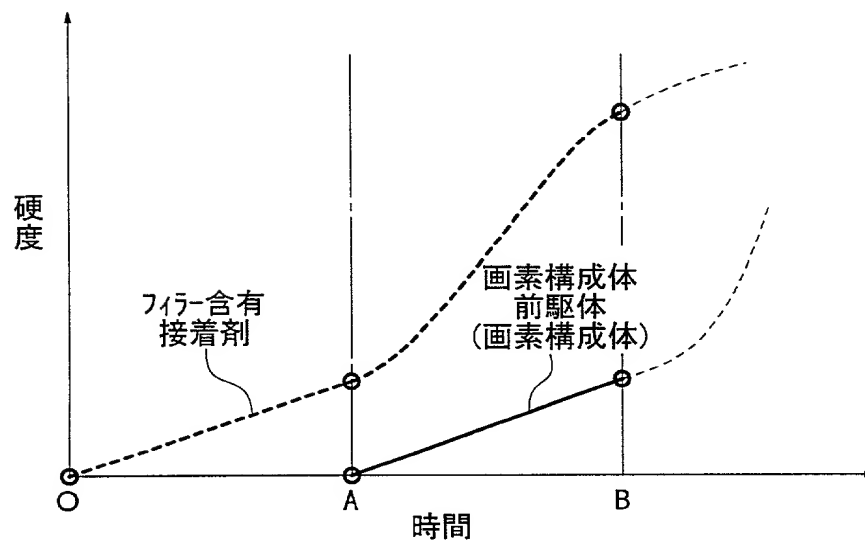


FIG. 16



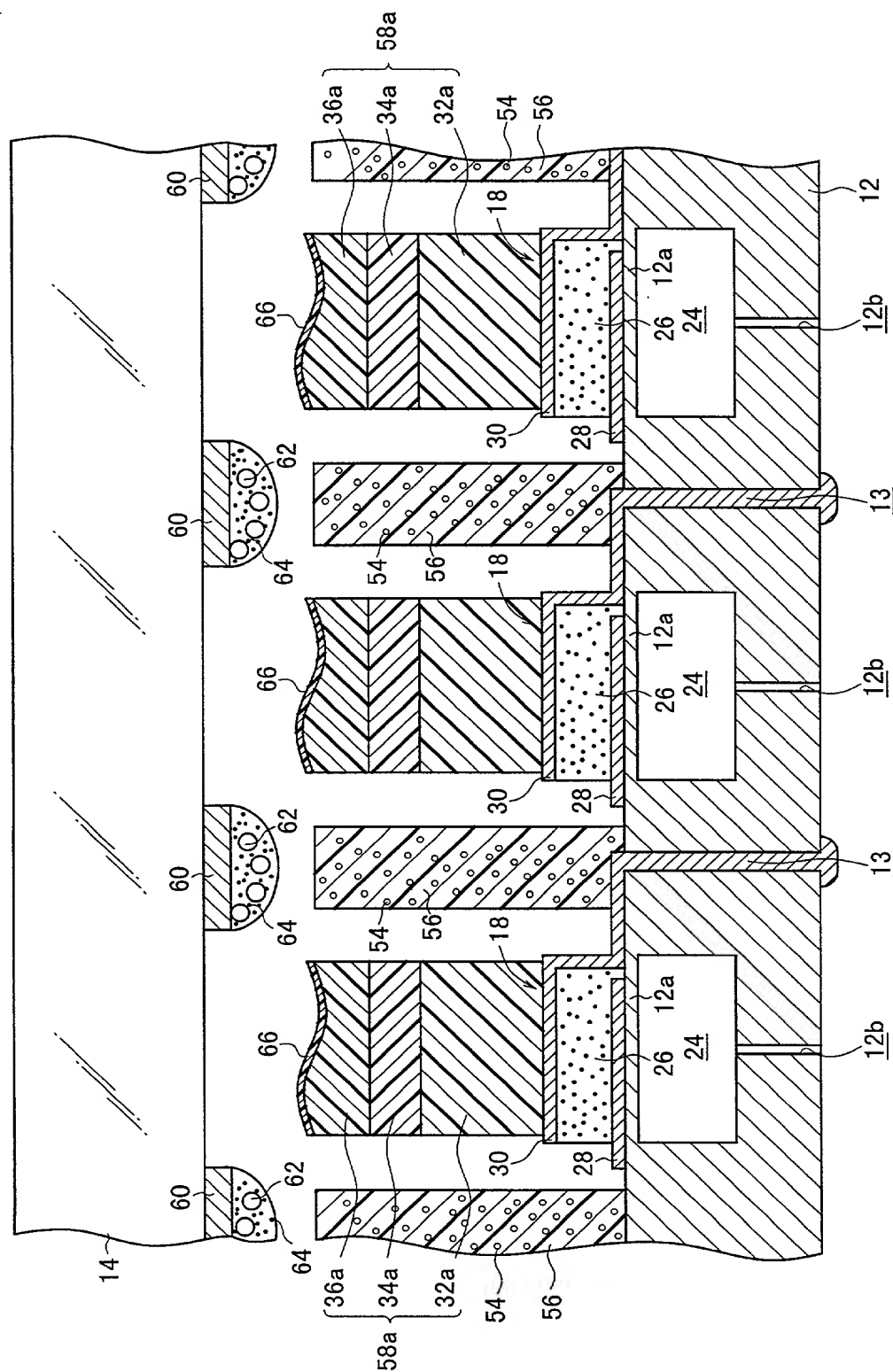
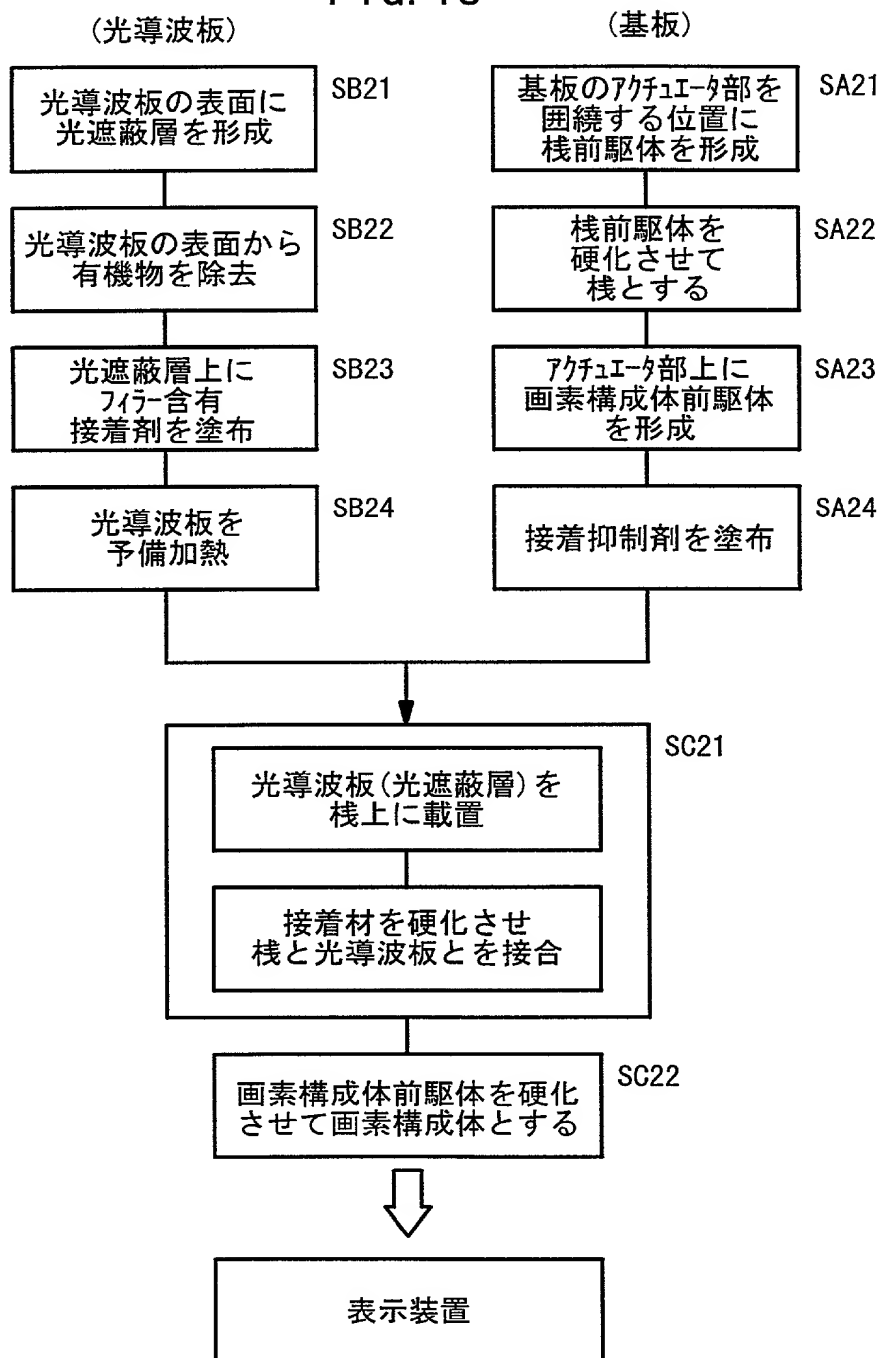


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FIG. 19

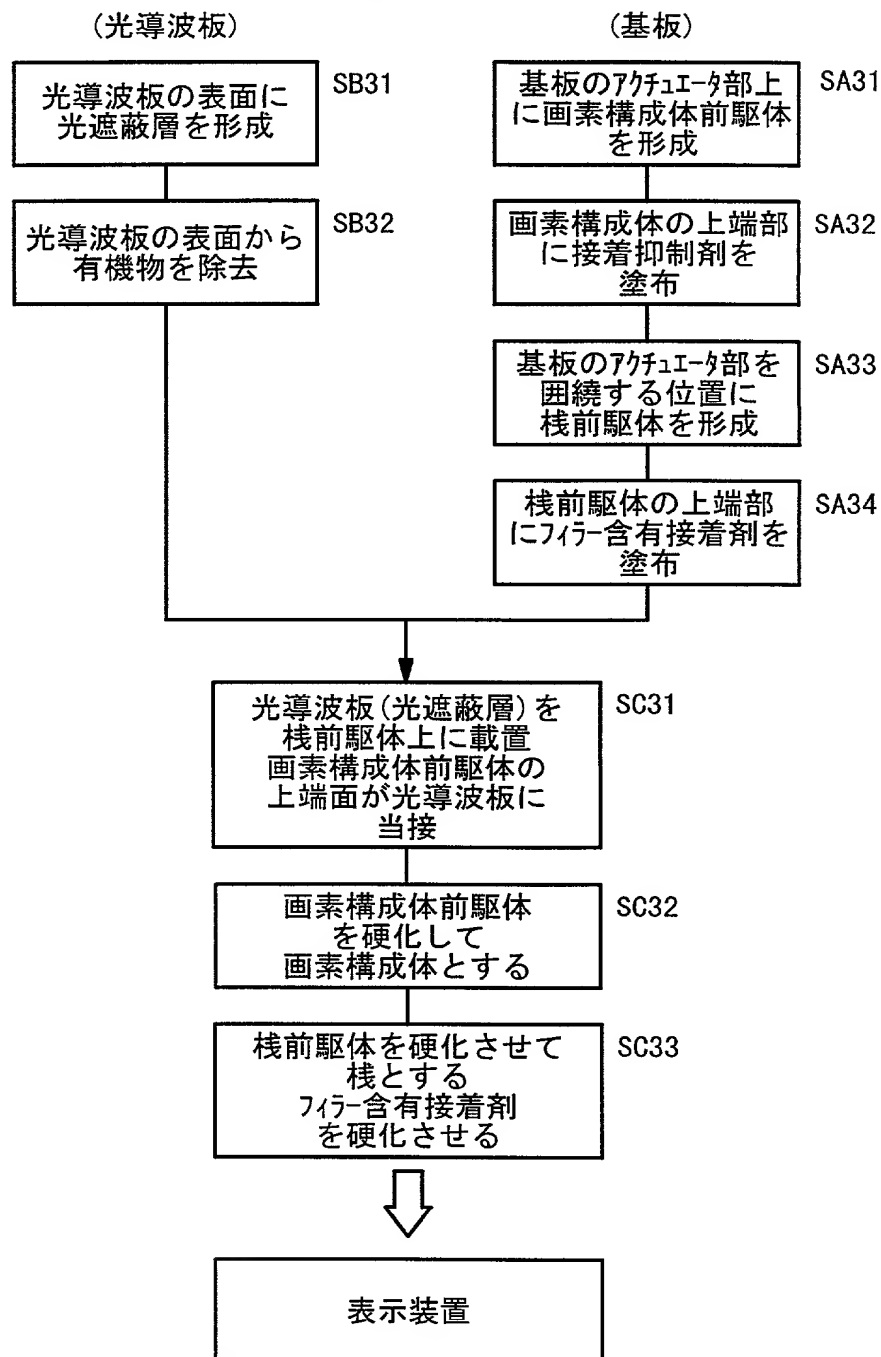
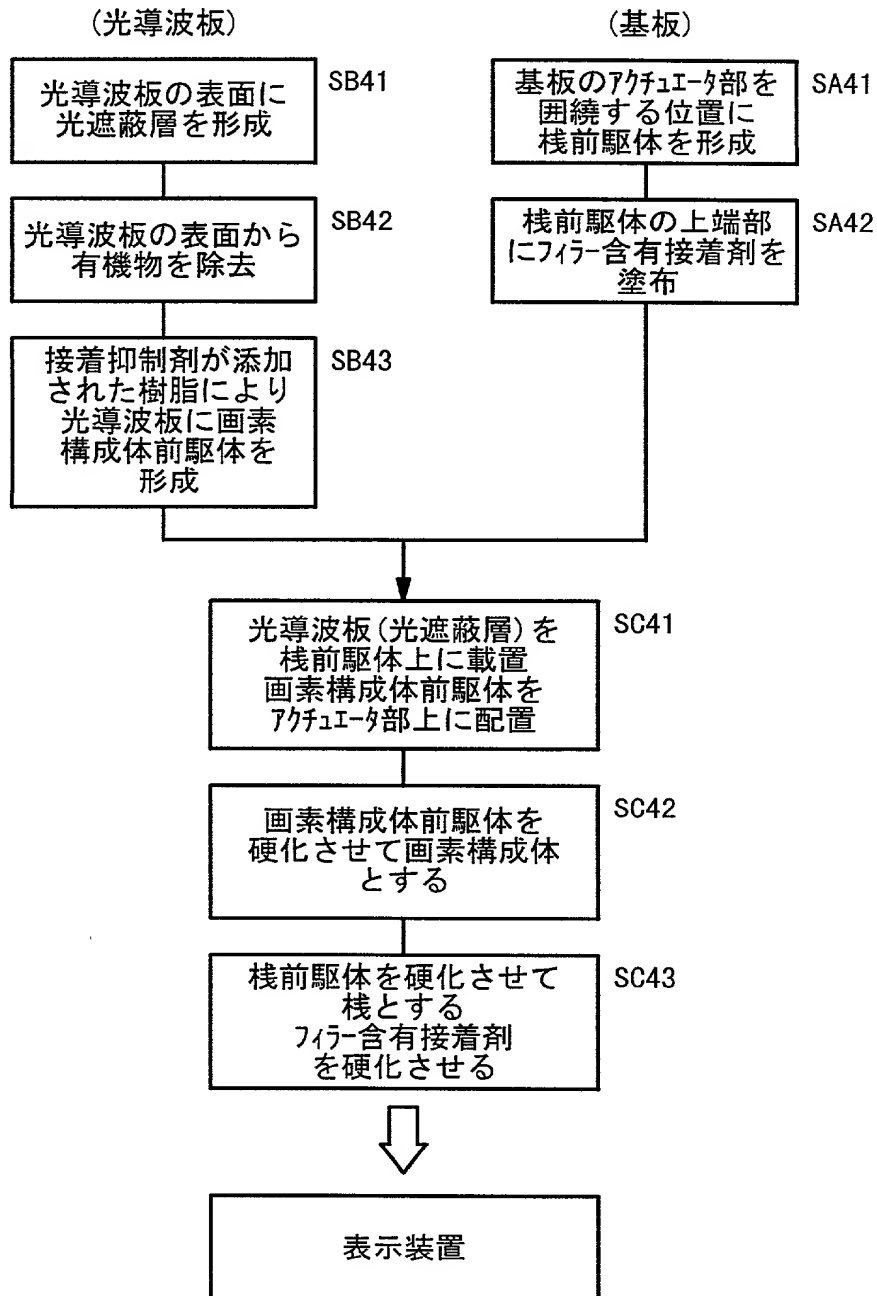


FIG. 20



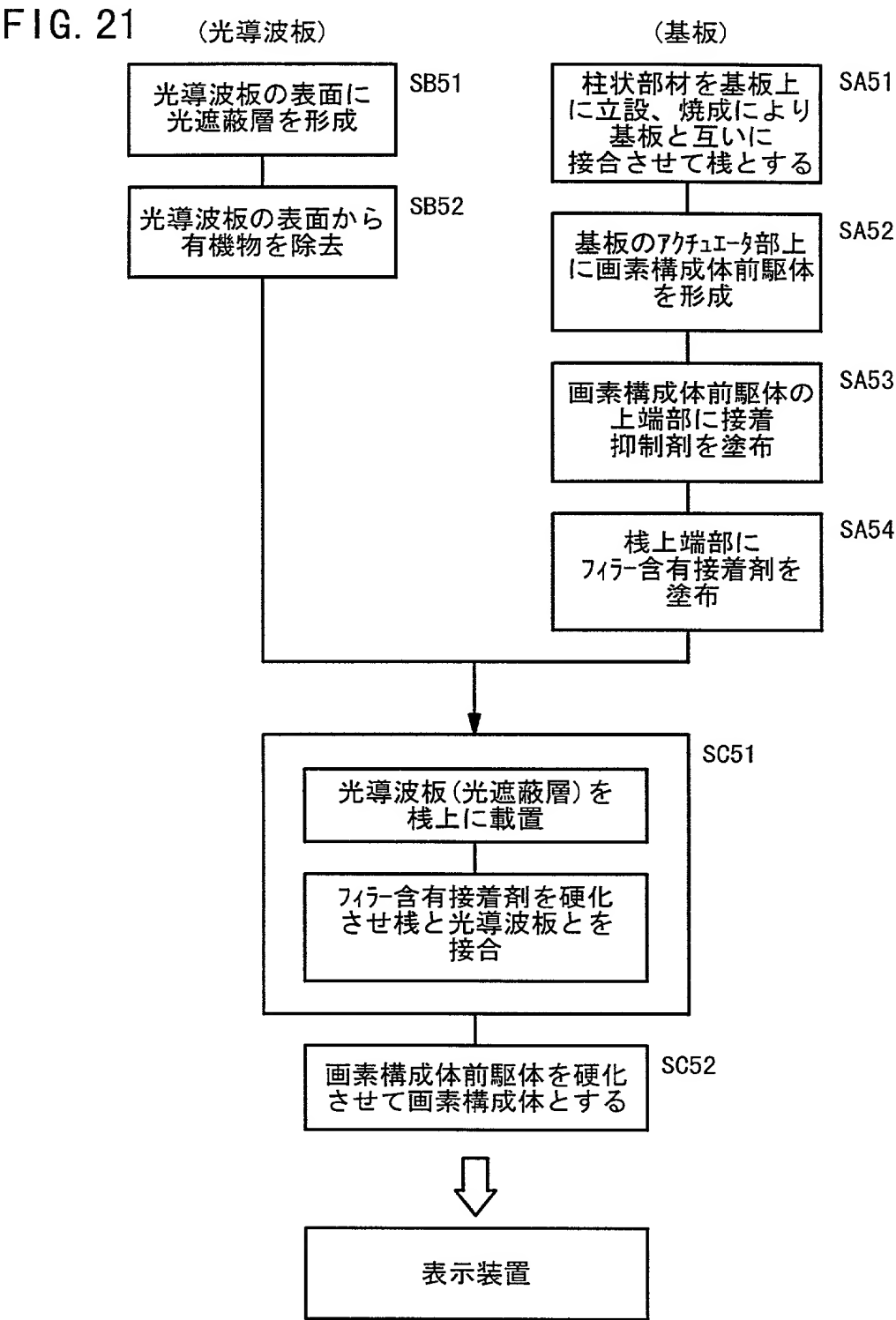


FIG. 22

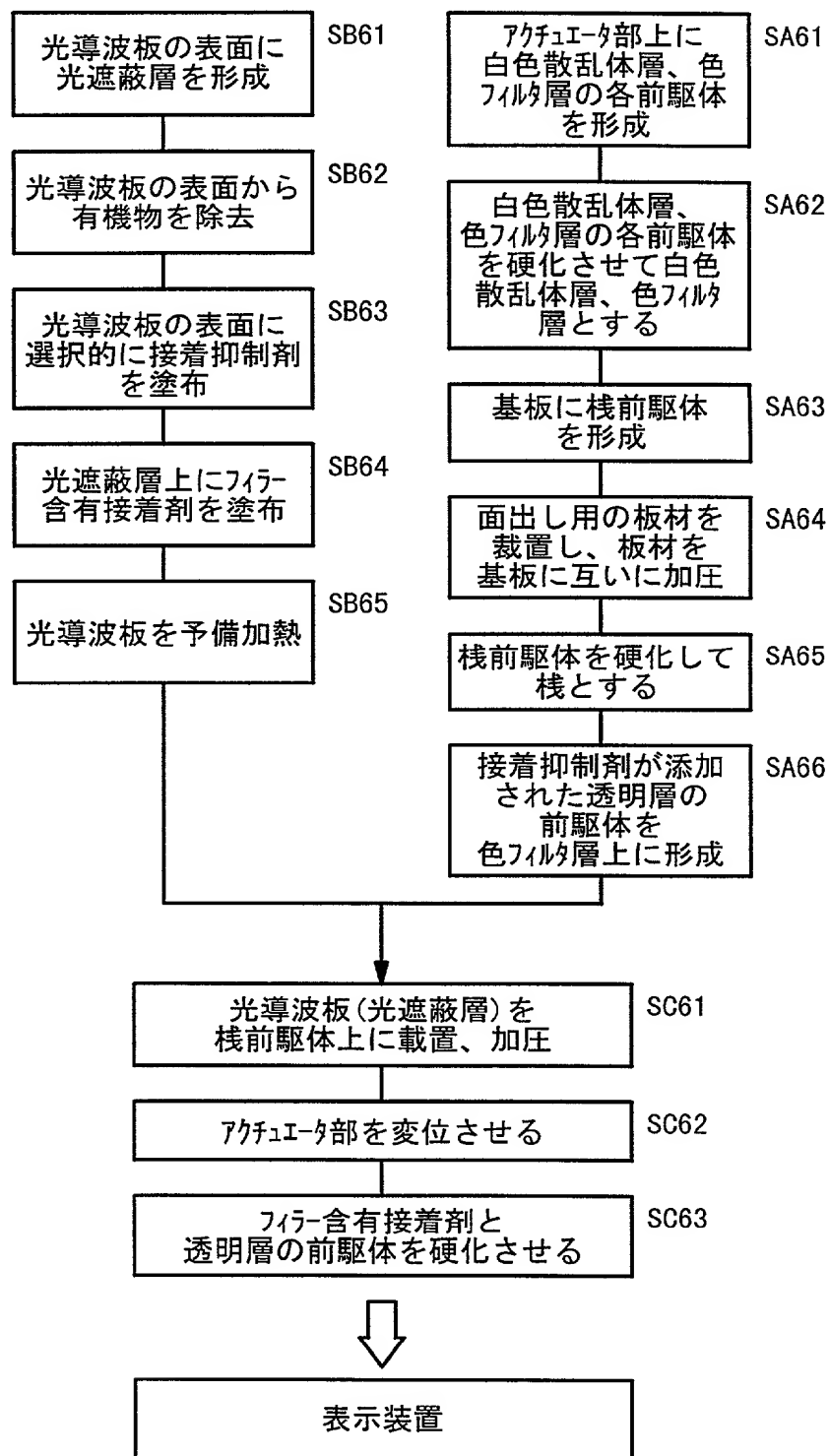


FIG. 23

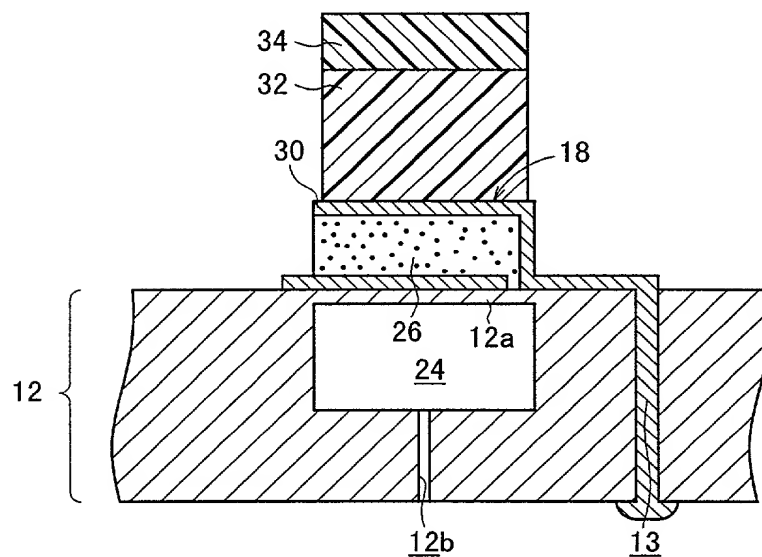
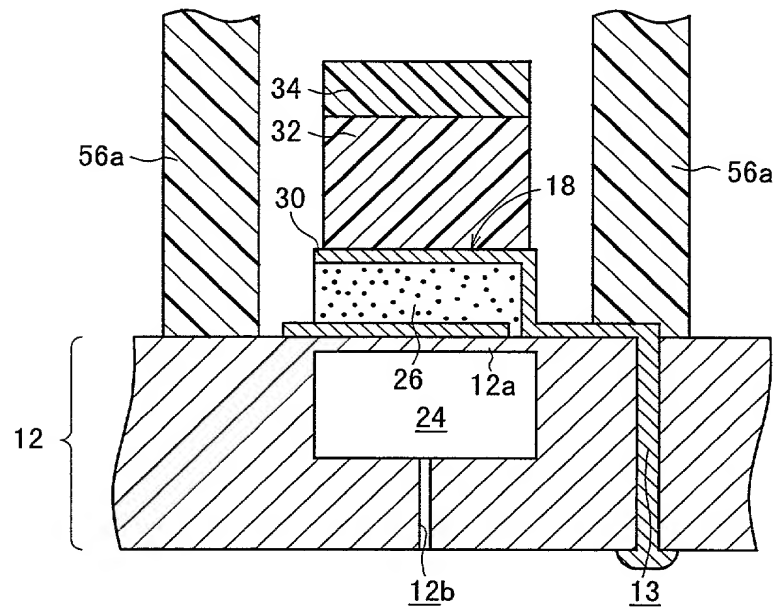
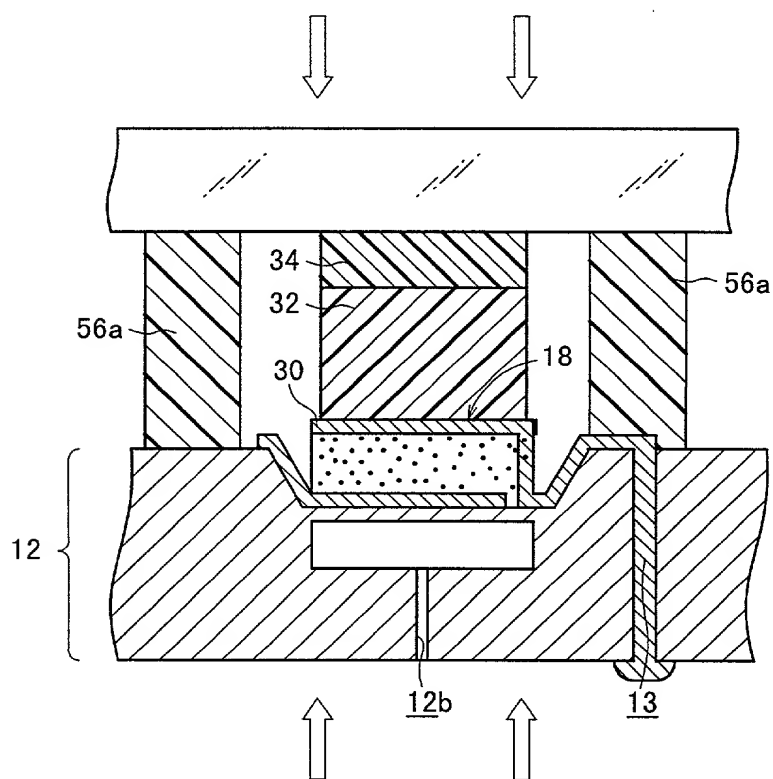
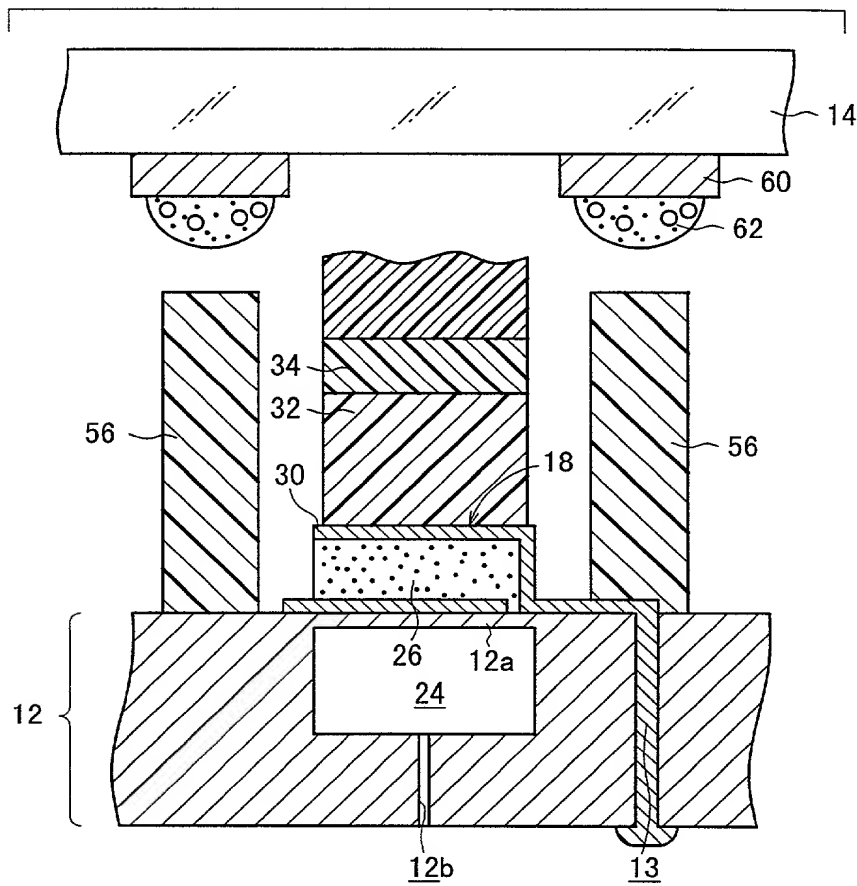


FIG. 24







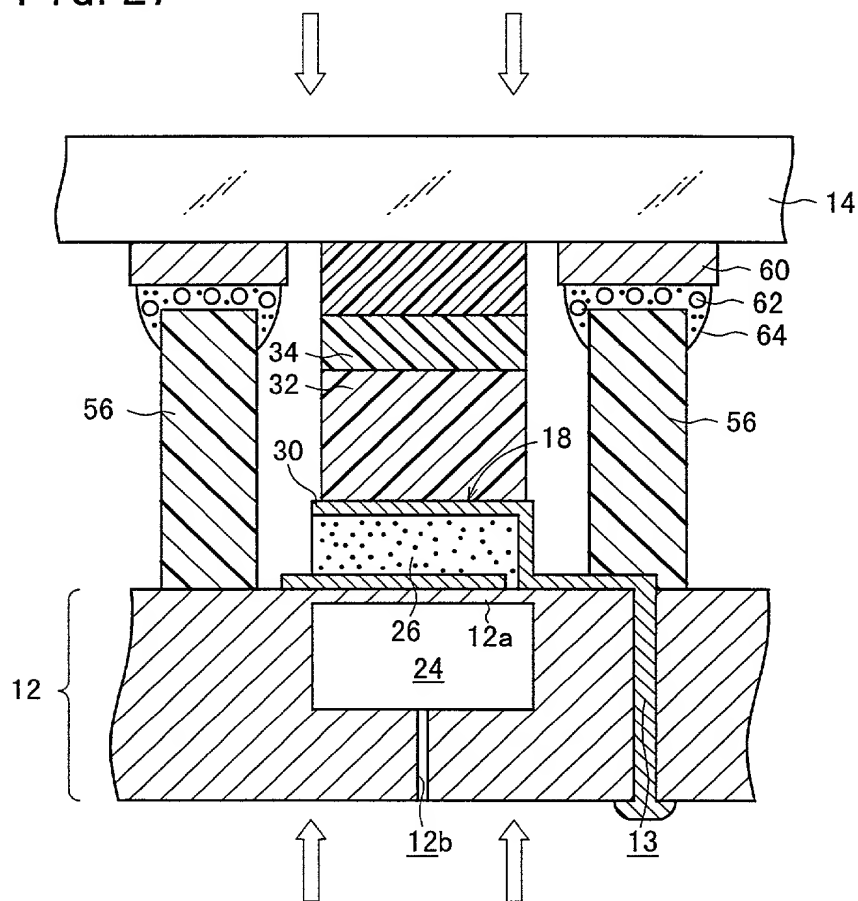
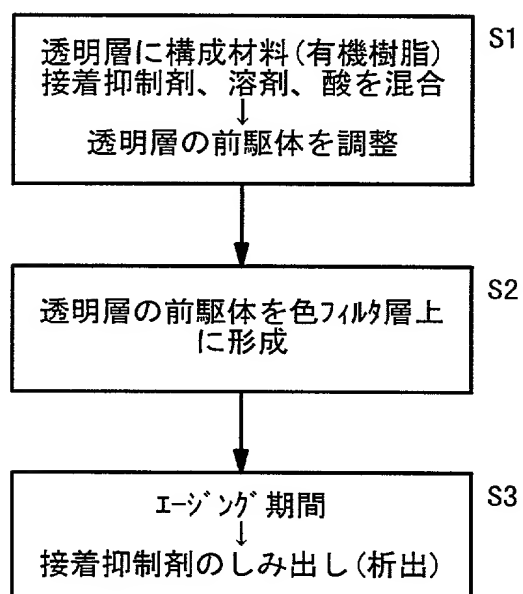


FIG. 28



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FIG. 29

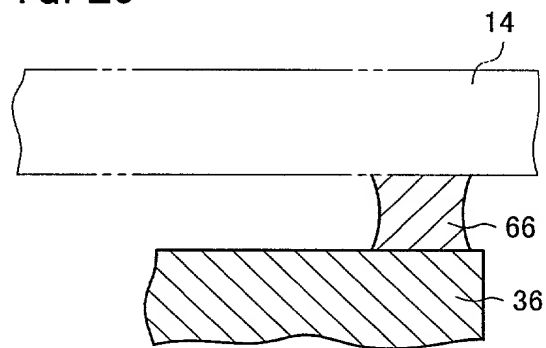


FIG. 30A

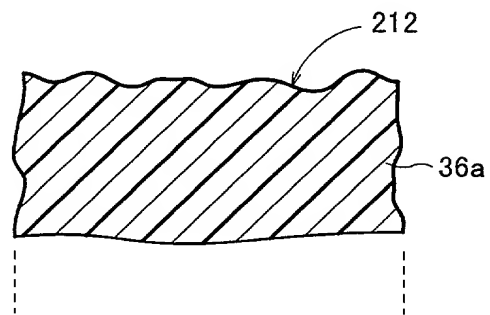


FIG. 30B

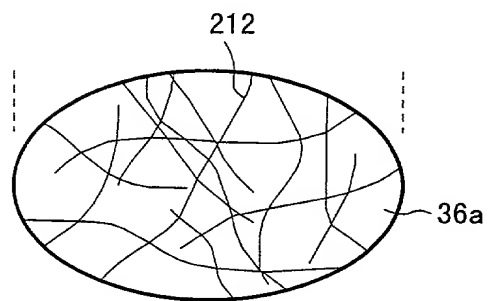


FIG. 31

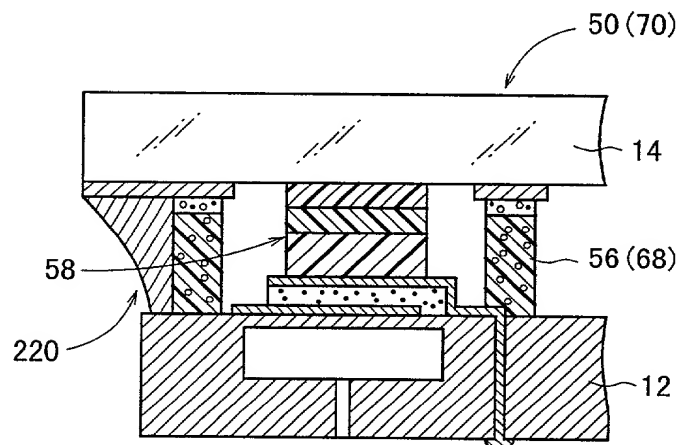
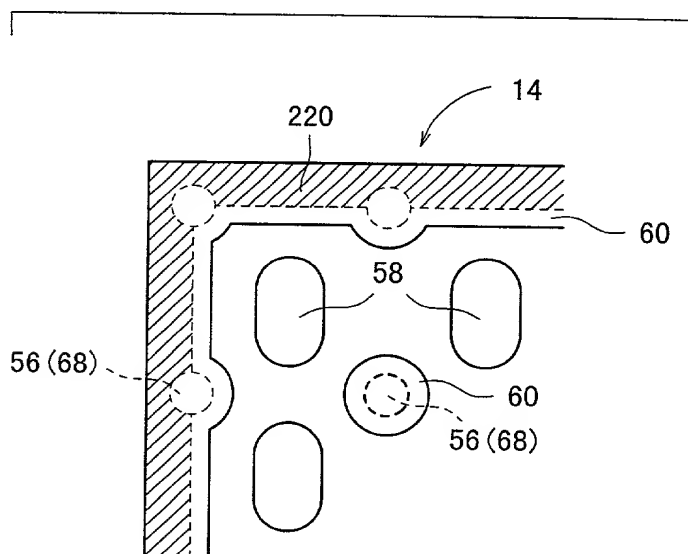


FIG. 32



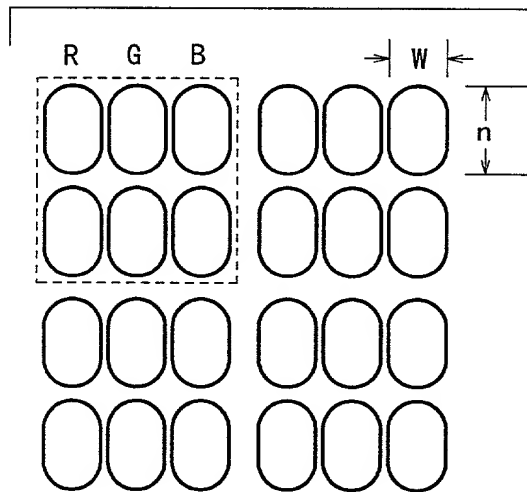
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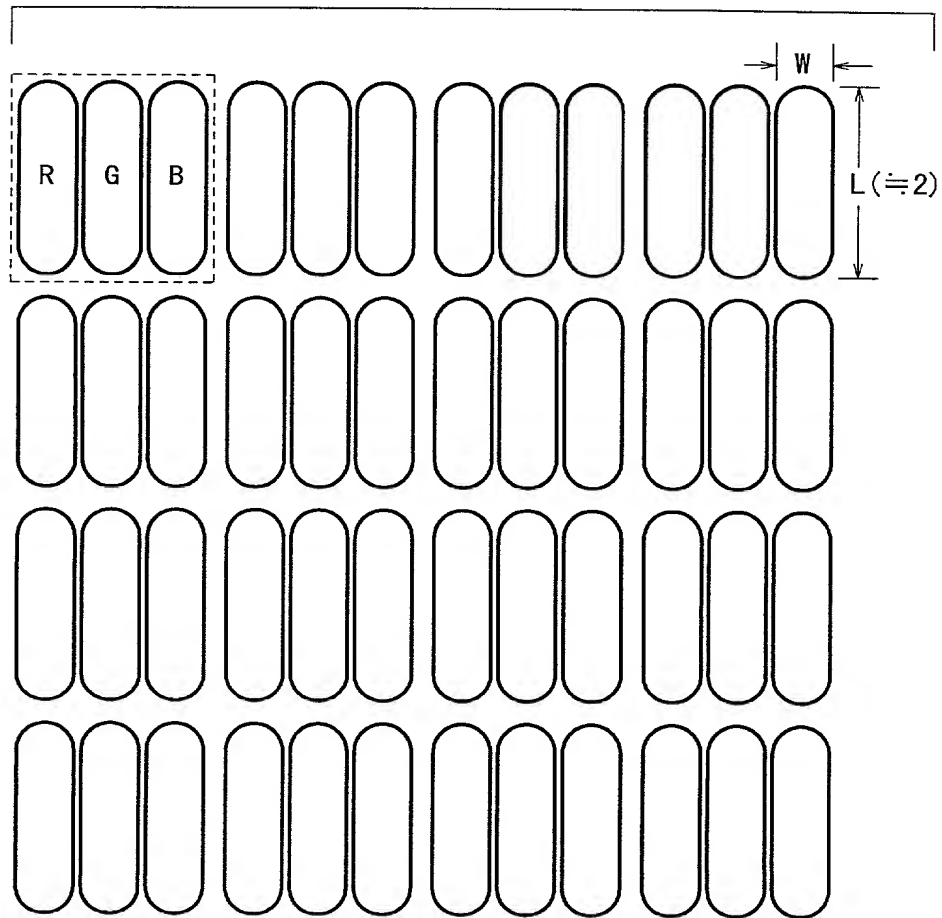
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FIG. 33



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FIG. 34



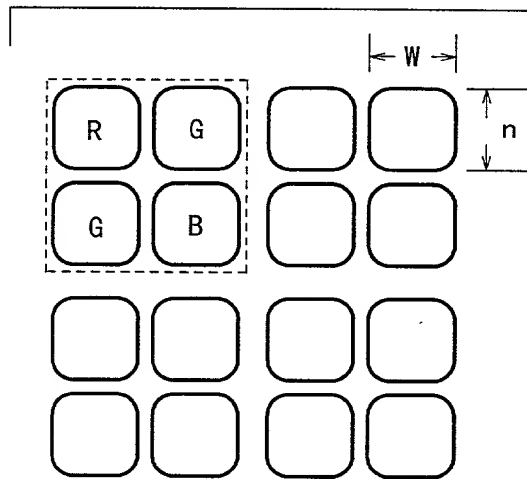
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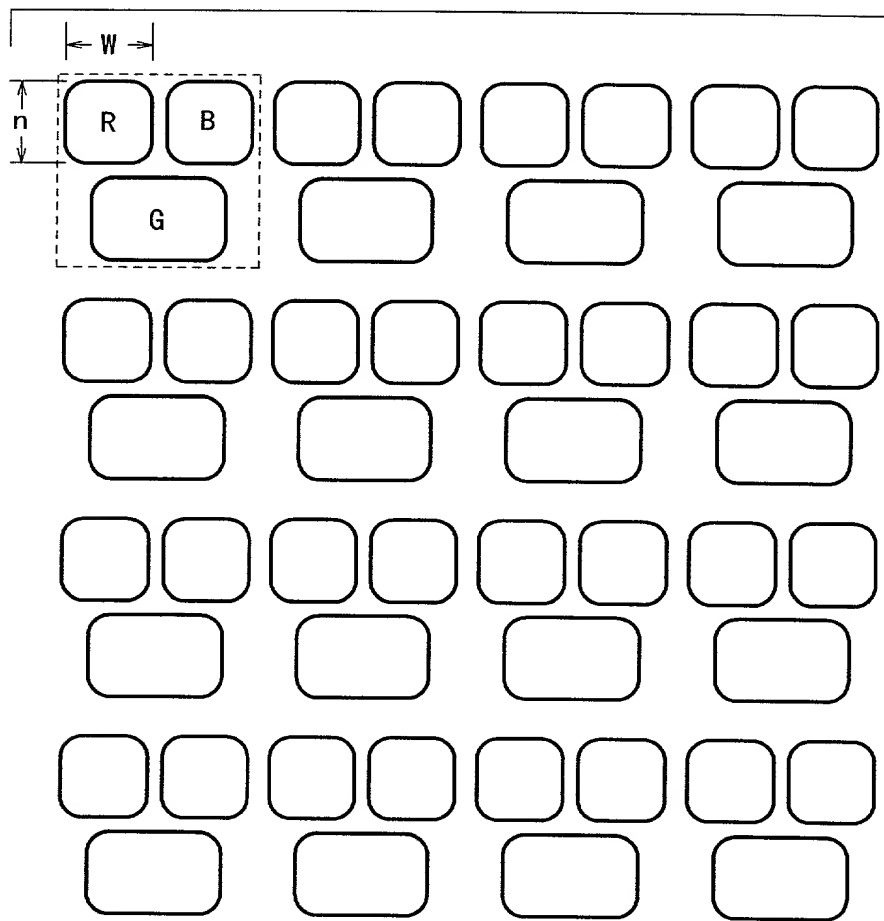
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FIG. 35



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FIG. 36



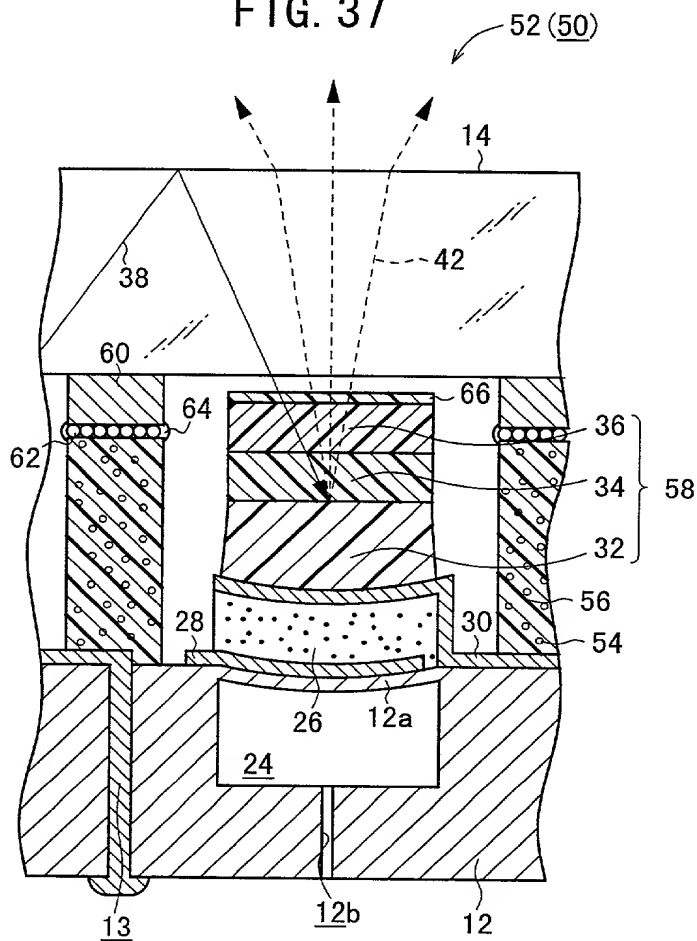


FIG. 38

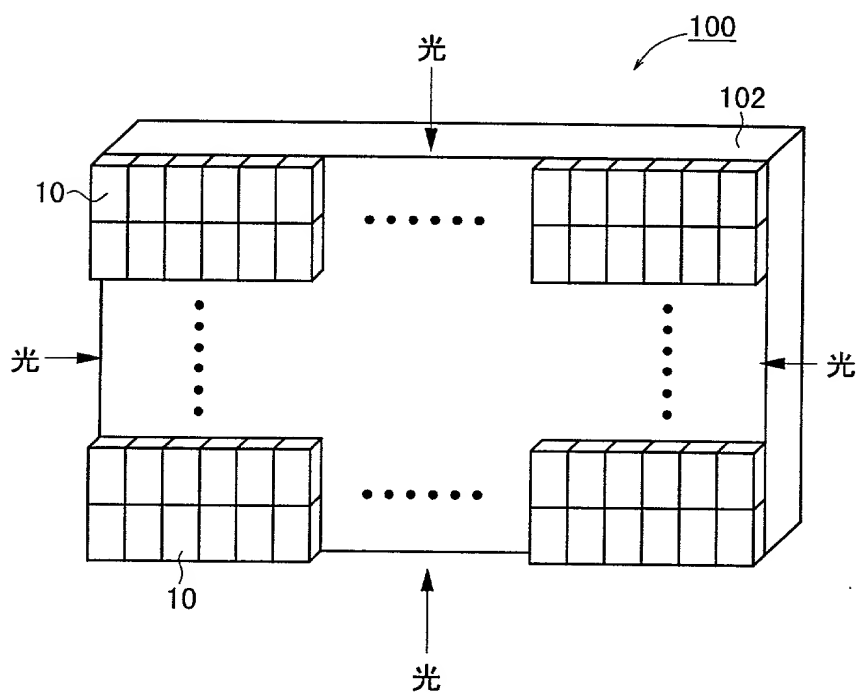
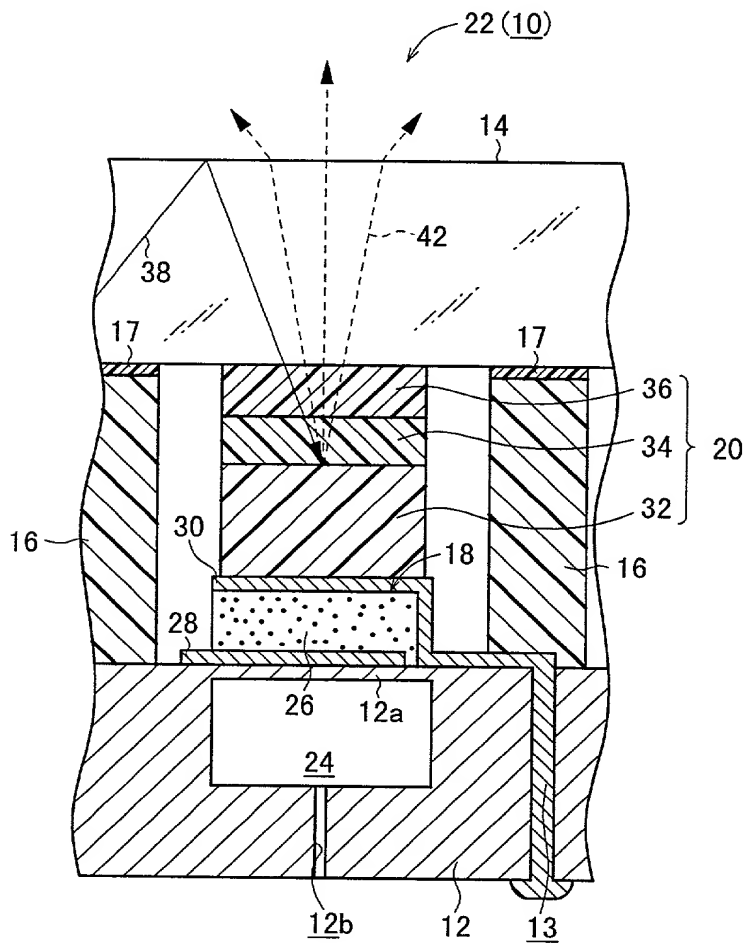


FIG. 39



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FIG. 40

